PATENT ABSTRACTS OF JAPAN

(11)Publication number : 11-233641

(43)Date of publication of application : 27.08.1999

(51)Int.Cl. H01L 21/8234
H01L 27/088
H01L 27/04
H01L 21/822
H01L 29/78

(21)Application number : 10-044577

(22)Date of filing : 10.02.1998

(71)Applicant : SEIKO EPSON CORP

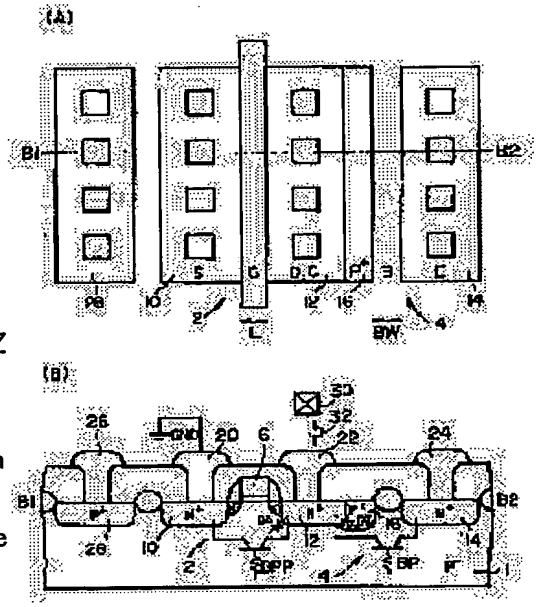
(72)Inventor : OKAWA KAZUHIKO
SAIKI TAKAYUKI

(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

(57)Abstract:

PROBLEM TO BE SOLVED: To make a semiconductor device compact, while ensuring a high ESD withstand voltage.

SOLUTION: An output transistor 2 has an N+ region 10 for a source region and an N+ region 12 for a drain region. A bipolar transistor 4 has an N+ region 12 for a collector region, a P well 1 for a base region and an N+ region 14 for an emitter region. A zener diode DZ composed of the junction of the N+ region 12 and a P+ region 16 is provided, and BP is set on-state instead of BPP, when a high voltage pulse 32 is imposed. A zener voltage VZ of the DZ is so controlled by an impurity density that the DZ is set lower than an avalanche breakdown voltage or a snap-back voltage in the drain region, and greater than an absolute maximum rated voltage. A gate length or a contact size, etc., is set as the minimum dimension on a design rule. A junction of the zener diode in a parallel direction with the surface of the semiconductor device is widened.



LEGAL STATUS

[Date of request for examination] 22.01.2002

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration] withdrawal

[Date of final disposal for application] 14.04.2003

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

CLAIMS

[Claim(s)]
[Claim 1] The FET transistor of the 2nd conductivity type which has a gate electrode while being formed in the 1st field of the 1st conductivity type, makes a source field the 1st impurity range of the 2nd conductivity type, and makes a drain field the 2nd impurity range of the 2nd conductivity type, The bipolar transistor which is formed in said 1st field, makes said 2nd impurity range a collector field, makes said 1st field a base region, and makes an emitter region the 3rd impurity range of said 2nd conductivity type separated from the 2nd impurity range by the component, The semiconductor device characterized by including the zener diode constituted by junction to the 4th impurity range of the 1st conductivity type which is a field contiguous to said 2nd impurity range, and is formed in the field between said 2nd and 3rd impurity range, and said 2nd impurity range.
[Claim 2] The semiconductor device with which zener voltage of said zener diode is characterized by being lower than the avalanche breakdown voltage in said drain field of said FET transistor in claim 1.
[Claim 3] The semiconductor device with which zener voltage of said zener diode is characterized by being lower than the snapback electrical potential difference in said drain field of said FET transistor in claim 1 or 2.
[Claim 4] The semiconductor device characterized by the zener voltage of said zener diode being more than an absolute-maximum-rating electrical potential difference of a semiconductor device lower than the electrical potential difference of either said avalanche breakdown voltage and said snapback electrical potential difference in claim 2 or 3.
[Claim 5] The semiconductor device with which said zener voltage is characterized by being controlled by high impurity concentration of said 4th impurity range in claim 1 thru/or either of 4.
[Claim 6] The semiconductor device characterized by the gate length of said gate electrode of said FET transistor having the lower limit on a design rule in claim 1 thru/or either of 5.
[Claim 7] In claim 1 thru/or either of 6 The size of drain contact of said drain field of said FET transistor, The distance of the 1st side of said drain contact, and the 3rd side by the side of said gate electrode of said drain field, Distance with the 4th side which intersects perpendicularly with the 2nd side of said drain contact, and said 3rd side of said drain field, The size of source contact of said source field of said FET transistor, The distance of the 5th side of said source contact, and the 7th side by the side of said gate electrode of said source field, The semiconductor device with which at least one of the distance with the 8th side which intersects perpendicularly with the 6th side of said source contact and said 7th side of said source field is characterized by having the lower limit on a design rule.
[Claim 8] The semiconductor device characterized by being larger than junction of the direction where the way of junction of an almost parallel direction crosses on the surface of a semiconductor device on the surface of a semiconductor device among junction to said 2nd impurity range and said four impurity ranges in claim 1 thru/or either of 7.

[Claim 9] The process which is the manufacture approach of the semiconductor device containing the FET transistor and bipolar transistor of the 2nd conductivity type, and forms the gate electrode of said FET transistor, The 1st impurity range of the 2nd conductivity type used as the source field of said FET transistor, The 2nd impurity range of the 2nd conductivity type used as the drain field of said FET transistor, and the collector field of said bipolar transistor, And the process which forms the 3rd impurity range of the 2nd conductivity type used as the emitter region of said bipolar transistor in the 1st field of the 1st conductivity type used as the base region of said bipolar transistor, The manufacture approach of the semiconductor device characterized by including the process which is a field contiguous to said 2nd impurity range, and forms in the field between said 2nd and 3rd impurity range the 4th impurity range of the 1st conductivity type which constitutes junction of zener diode with said 2nd impurity range.
[Claim 10] The manufacture approach of the semiconductor device characterized by making the impurity placing field for forming the impurity placing field and said 4th impurity range for forming said 2nd impurity range so that the way of junction of an almost parallel direction may become larger than junction of the direction which crosses on the surface of a semiconductor device on the surface of a semiconductor device in claim 9 among junction to said 2nd impurity range and said four impurity ranges overlap.
[Claim 11] The manufacture approach of the semiconductor device characterized by forming said 4th impurity range in the field estranged from the front face of a semiconductor device in claim 9 or 10.
[Claim 12] The manufacture approach of the semiconductor device characterized by forming in one process of the processes which form the source field and drain field of an FET transistor of the process which forms a low concentration impurity range [in / for said 4th impurity range / the LDD structure of the FET transistor of the 1st conductivity type], and the 1st conductivity type in claim 9 thru/or either of 11.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the structure of protecting a circuit from surges, such as static electricity, about a semiconductor device.
[0002]
Background Art and Problem(s) to be Solved by the Invention] In a semiconductor device, it is necessary to raise ESD susceptibility so that the electrostatic discharge of the internal circuitry etc. may not be carried out by surges, such as static electricity. And the technique indicated by IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL.44, NO.7, JULY 1997, and JP,7-202126,A as a background technique which raises ESD susceptibility is known. This background technique is explained using drawing 1 (A) and (B). In addition, drawing 1 (A) is the top view of this background technique, and drawing 1 (B) is a sectional view in A1-A2 line of drawing 1 (A).
[0003] In drawing 1 (A) and (B), the output transistor 202 and the bipolar transistor (BP) 204 are formed in the P well 201 formed in the semi-conductor substrate. The output transistor 202 which is MOSFET of the LDD (Lightly Doped Drain) structure of N type has the gate electrode 206, and makes the source field and the N+ field 212 the drain field for the N+ field 210. Moreover, a bipolar transistor (BP) 204 makes the N+ field 212 a collector field, and makes the base region and the N+ field 214 the emitter region for the P well 201. The N+ field 210 is connected to a GND line (touch-down potential) through a wiring layer 220 here. Moreover, the N+ field 212 is connected to pads 230 (an output terminal, an input/output terminal, input terminal, etc.) through a wiring layer 222. Moreover, the N+ field 214 is connected to a GND line or a given discharge line through a wiring layer 224. Moreover, the P well 201 is connected to a GND line or a discharge line through the P+ field 228 (well tap) and a wiring layer 226.
[0004] The description of this example of a background is that it made gate length (effective channel length) L of the output transistor 202 longer than the base width of face (effective base width of face) BW of a bipolar transistor (BP) 204. When the high-tension pulse (surge) 232 is impressed to a pad 230, BP can be made to turn on by doing in this way instead of the parasitism bipolar transistor BPP constituted by the N+ field 212, the P well 201, and the N+ field 210. Consequently, it can prevent that a high current flows to BPP, and can prevent now that the electrostatic discharge of the output transistor 202 (especially gate dielectric film) is carried out.
[0005] However, there is a problem that gate length L is not made to the lower limit on a design rule in this background technique. When [which is the lower limit on a design rule about the base width of face BW] it is made 0.8 micrometers, for example, gate length L must be set to 1.8 micrometers. And if gate length L becomes long in this way, the current serviceability of the output transistor 202 will decline.
[0006] On the other hand, in order to heighten current serviceability, with gate length L lengthened, it is necessary to lengthen gate width W, and this causes the result of large-scale-izing of the layout area of the output transistor 202. Since many pads (an output pad, an I/O pad, input pad, etc.) are dramatically prepared in a semiconductor device in recent years, large-scale-ization of the layout area of the output transistor 202 causes the result of large-scale-izing of a chip area, or the cost rise of a semiconductor

device.
[0007] The place which it is made in order that this invention may solve the above technical problems, and is made into the object is to offer the semiconductor device which can realize small-scale-ization of a chip area, and its manufacture approach, securing high ESD susceptibility.
[0008]
[Means for Solving the Problem] The semiconductor device applied to this invention in order to solve the above-mentioned technical problem The FET transistor of the 2nd conductivity type which has a gate electrode while being formed in the 1st field of the 1st conductivity type, makes a source field the 1st impurity range of the 2nd conductivity type, and makes a drain field the 2nd impurity range of the 2nd conductivity type, The bipolar transistor which is formed in said 1st field, makes said 2nd impurity range a collector field, makes said 1st field a base region, and makes an emitter region the 3rd impurity range of said 2nd conductivity type separated from the 2nd impurity range by the component, It is characterized by including the zener diode constituted by junction to the 4th impurity range of the 1st conductivity type which is a field contiguous to said 2nd impurity range, and is formed in the field between said 2nd and 3rd impurity range, and said 2nd impurity range.
[0009] According to this invention, if the high-tension pulse by ESD etc. is impressed to the 2nd impurity range, before the parasitism diode constituted by junction to the 2nd impurity range and the 1st field will carry out avalanche breakdown, Zener breakdown of the zener diode constituted by junction to the 2nd impurity range and the 4th impurity range can be carried out. Thereby, the surge current by a high-tension pulse etc. can be discharged now by the bipolar transistor constituted by the 2nd impurity range, the 1st field, and the 3rd impurity range. Therefore, it becomes possible to be able to prevent that a high current flows to the parasitism bipolar transistor (bipolar transistor which is parasitic on an FET transistor) constituted by the 2nd impurity range, the 1st field, and the 1st impurity range, and to raise ESD susceptibility to it. In addition, there is no constraint that gate length must be made longer than the base width of face of a bipolar transistor in this invention, and gate length can be shortened. consequently, according to this invention, securing high ESD susceptibility, a semiconductor device is boiled markedly and it can miniaturize.
[0010] Moreover, it is characterized by the zener voltage of this invention of said zener diode being lower than the avalanche breakdown voltage in said drain field of said FET transistor. By doing in this way, before the parasitism diode of a drain field carries out avalanche breakdown, it becomes possible to carry out Zener breakdown of the zener diode certainly.
[0011] Moreover, it is characterized by the zener voltage of this invention of said zener diode being lower than the snapback electrical potential difference in said drain field of said FET transistor.
[0012] By doing in this way, it is stabilized through a bipolar transistor and the surge current by a high-tension pulse etc. can be discharged now.
[0013] Moreover, this invention is characterized by the zener voltage of said zener diode being more than an absolute-maximum-rating electrical potential difference of a semiconductor device lower than the electrical potential difference of either said avalanche breakdown voltage and said snapback electrical potential difference. By doing in this way, the leakage current in the drain field at the time of normal operation can be reduced effectively, realizing reservation of high ESD susceptibility, and miniaturization of a semiconductor device.
[0014] Moreover, this invention is characterized by controlling said zener voltage by high impurity concentration of said 4th impurity range. By doing in this way, control which makes zener voltage a desired value can be simply realized now.
[0015] Moreover, as for this invention, gate length of said gate electrode of said FET transistor is characterized by having the lower limit on a design rule. By doing in this way, the current serviceability of FET transistor sufficient with short gate width can be obtained now. That is, miniaturization of a semiconductor device can be attained, maintaining the current serviceability of an FET transistor.
[0016] This invention Moreover, the size of drain contact of said drain field of said FET transistor, The

distance of the 1st side of said drain contact, and the 3rd side by the side of said gate electrode of said drain field, Distance with the 4th side which intersects perpendicularly with the 2nd side of said drain contact, and said 3rd side of said drain field, The size of source contact of said source field of said FET transistor, At least one of the distance of the 5th side of said source contact and the 7th side by the side of said gate electrode of said source field and the distance with the 8th side which intersects perpendicularly with the 6th side of said source contact and said 7th side of said source field is characterized by having the lower limit on a design rule. By doing in this way, a semiconductor device can be further miniaturized now.

[0017] Moreover, this invention is characterized by being larger than junction of the direction where the way of junction of an almost parallel direction crosses on the surface of a semiconductor device on the surface of a semiconductor device among junction to said 2nd impurity range and said four impurity ranges. Area of the whole junction of zener diode can be enlarged and it comes to be able to enlarge current passage area of the surge current in a discharge path by doing in this way. Consequently, it becomes possible to raise ESD susceptibility further.

[0018] Moreover, the process which this invention is the manufacture approach of the semiconductor device containing the FET transistor and bipolar transistor of the 2nd conductivity type, and forms the gate electrode of said FET transistor, The 1st impurity range of the 2nd conductivity type used as the source field of said FET transistor, The 2nd impurity range of the 2nd conductivity type used as the drain field of said FET transistor, and the collector field of said bipolar transistor, And the process which forms the 3rd impurity range of the 2nd conductivity type used as the emitter region of said bipolar transistor in the 1st field of the 1st conductivity type used as the base region of said bipolar transistor, It is characterized by including the process which is a field contiguous to said 2nd impurity range, and forms in the field between said 2nd and 3rd impurity range the 4th impurity range of the 1st conductivity type which constitutes junction of zener diode with said 2nd impurity range.

[0019] According to this invention, it becomes possible to form a compact semiconductor device with high ESD susceptibility. In addition, the process which forms the 4th impurity range may be performed before the process which forms the 1st, 2nd, and 3rd impurity range, and may be performed behind.

[0020] Moreover, this invention is characterized by making the impurity placing field for forming the impurity placing field and said 4th impurity range for forming said 2nd impurity range overlap so that the way of junction of an almost parallel direction may become larger than junction of the direction which crosses on the surface of a semiconductor device on the surface of a semiconductor device among junction to said 2nd impurity range and said four impurity ranges. If it does in this way, area of the whole junction of zener diode can be enlarged only by enlarging the overlap of impurity placing fields, and it will become possible to raise ESD susceptibility further.

[0021] Moreover, this invention is characterized by forming said 4th impurity range in the field estranged from the front face of a semiconductor device. By doing in this way, it can prevent now that the 4th impurity range is exposed on the surface of a semiconductor device.

[0022] Moreover, this invention is characterized by forming in one process of the processes which form the source field and drain field of an FET transistor of the process which forms a low concentration impurity range [in / for said 4th impurity range / the LDD structure of the FET transistor of the 1st conductivity type], and the 1st conductivity type. By doing in this way, a routing counter can be reduced and shortening of the manufacture period of a semiconductor device and low cost-ization of a semiconductor device can be attained.

[0023]

[Embodiment of the Invention] Hereafter, the good operation gestalt of this invention is explained. In addition, below, the 1st conductivity type is used as P type, and the 2nd conductivity type is explained as N type. Moreover, the example of application to electrostatic-discharge prevention of the output transistor of an MOS mold is explained. However, this invention can be applied, also when the 1st conductivity type is N type and the 2nd conductivity type is P type. Moreover, besides a MOS transistor,

it is applicable to various FET transistors, such as an MIS mold transistor. Furthermore, it is applicable to the transistor prepared as a protection network of an input pad besides an output transistor.

[0024] 1. An example of the top view of this operation gestalt is shown in the block diagram 2 of this operation gestalt (A). Moreover, the sectional view of the B1–B–2 line in drawing 2 (A) is shown in drawing 2 (B).

[0025] In drawing 2 (A) and (B), the output transistor 2 and the bipolar transistor (BP) 4 are formed in the P well 1 (the 1st field of the 1st conductivity type) formed in the semi–conductor substrate. The output transistor (output buffer) 2 which is MOSFET of the LDD (Lightly Doped Drain) structure of N type has the gate electrode 6, and makes the drain field the source field and the N+ field 12 (the 2nd impurity range of the 2nd conductivity type) for the N+ field 10 (the 1st impurity range of the 2nd conductivity type). Moreover, a bipolar transistor (BP) 4 makes the above–mentioned N+ field 12 a collector field, and makes the emitter region the base region and the N+ field 14 (the 3rd impurity range of the 2nd conductivity type) for the P well 1. That is, the N+ field 12 is used as a drain field with the output transistor 2, and is used as a collector field by the bipolar transistor 4 (shared by the output transistor 2 and the bipolar transistor 4).

[0026] The N+ field 10 is connected to a GND line (touch–down potential) through a wiring layer 20 here. Moreover, the N+ field 12 is connected to pads 30 (an output terminal, an input/output terminal, input terminal, etc.) through a wiring layer 22. Moreover, the N+ field 14 is connected to a GND line or a given discharge line through a wiring layer 24. Moreover, the P well 1 is connected to a GND line or a discharge line through the P+ field 28 (well tap) and a wiring layer 26.

[0027] In addition, below, the source field 10, and a call and the N+ field 12 are suitably made to call suitably the drain field 12 or the collector field 12, and a call and the N+ field 14 an emitter region 14 for the N+ field 10.

[0028] The description of this operation gestalt is in the point of being a field contiguous to the N+ field 12, and having established the P+ field 16 (the 4th impurity range of the 1st conductivity type) in the field between the N+ field 12 and the N+ field 14 so that it may understand, if drawing 1 (A) and (B) are compared with drawing 2 (A) and (B). That is, it is in the point of having formed the zener diode DZ constituted by junction to the N+ field 12 and the P+ field 16. When doing in this way and the high–tension pulse 32 is impressed to a pad 30, before the parasitism diode DA constituted by junction to the N+ field 12 and the P well 1 carries out avalanche breakdown, it becomes possible to carry out Zener breakdown of the zener diode DZ. Thereby, BP can be made to turn on instead of the parasitism bipolar transistor BPP constituted by the N+ field 12, the P well 1, and the N+ field 10. Consequently, it can prevent that a high current flows to BPP, and can prevent now that the electrostatic discharge of the output transistor 2 (especially gate dielectric film) is carried out.

[0029] And in the example of a background of drawing 1 (A) and (B), if gate length L was not made longer than the base width of face BW, BP could not be made to turn on instead of BPP, and gate length was not made to the lower limit on a design rule. On the other hand, BP can be made to turn on instead of BPP according to this operation gestalt, making gate length L into the lower limit on a design rule. Consequently, securing high ESD susceptibility, layout area of the output transistor 2 can be made small, and miniaturization of a semiconductor device and low cost–ization can be attained.

[0030] 2. With the usual output transistor in which the setting–out zener diode DZ of zener voltage is not formed, if a high–tension pulse (surge) is impressed to a drain field, the parasitism diode DA of a drain field will carry out avalanche breakdown. At this time, as shown in E1 of drawing 3 , a drain electrical potential difference is set to VAB (avalanche breakdown voltage). Then, ON of the parasitism bipolar transistor BPP reduces a drain electrical potential difference to VSB (snapback electrical potential difference) from VAB, as shown in E2 of drawing 3 . Thus, the phenomenon in which a drain electrical potential difference falls is called a snapback.

[0031] He is trying for the zener voltage VZ of zener diode DZ to become lower than the avalanche breakdown voltage VAB in the drain field 12 of the output transistor 2 with this operation gestalt, as

shown in E3 of drawing 3 (VZ<VAB). By doing in this way, before DA carries out avalanche breakdown, it becomes possible to carry out Zener breakdown of the DZ certainly, and it becomes possible to make BP turn on instead of being BPP.

[0032] Furthermore, it is made for zener voltage VZ to become lower than the snapback electrical potential difference VSB in the drain field 12 of the output transistor 2 preferably, as shown in E4 of drawing 3 (VZ<VSB). By doing in this way, it is stabilized in a bipolar transistor BP side, and a current can be discharged now. Namely, by setting it as VZ<VSB, a drain electrical potential difference can be clamped now on an electrical potential difference lower than the snapback electrical potential difference VSB at the time of high-tension pulse impression. Thus, if a drain electrical potential difference can be clamped on an electrical potential difference lower than VSB, also when DA will have carried out avalanche breakdown by a certain factor, it can guarantee certainly that BPP does not turn on. Consequently, it can prevent effectively that the discharge path of a current changes to the BPP side from the BP side, and the electrostatic discharge of the output transistor 2 can be certainly prevented now.

[0033] Moreover, as shown in E3 of drawing 3 , or E4, as for the zener voltage VZ of DZ, it is desirable to become more than the absolute-maximum-rating electrical potential difference VAM of a semiconductor device. That is, it is desirable to become VAB>VZ>=VAM or VSB>VZ>=VAM. By doing in this way, it can prevent that leakage current flows from the drain field 12 through zener diode DZ to the P well 1 at the time of normal operation, securing high ESD susceptibility.

[0034] Usually, adjoining the drain field 12, forming the P+ field 16, and forming zener diode DZ is not considered as a desirable design. It is because leakage current may flow through DZ. This operation gestalt has the description in the point of having adjoined the drain field 12 daringly against the situation used as the hindrance of constituting such this operation gestalt, having formed the P+ field 16, and having prepared DZ. That is, if zener voltage VZ is adjusted so that it may become more than the absolute-maximum-rating electrical potential difference VAM, the description is in the point of having prepared DZ paying attention to the ability preventing leakage current flowing at the time of normal operation. And if VZ is adjusted so that it may become VZ>=VAM and may become VZ<VAB or VZ<VSB, ESD susceptibility can be raised at the time of high-tension pulse impression, preventing leakage current at the time of normal operation.

[0035] 3. The zener voltage VZ of drawing 3 is controlled by the control book operation gestalt of zener voltage with the high impurity concentration of the P+ field 16. Thereby, zener voltage VZ can be controlled now to become VAB>VZ>=VAM or VSB>VZ>=VAM.

[0036] The example of distribution with a high impurity concentration of Y= 0.1 micrometers [at the time of taking a Y-axis in the direction which intersects perpendicularly in the direction which meets drawing 4 (A) on the surface of a semiconductor device like drawing 4 (B) at the X-axis and the X-axis] is shown. Junction of zener diode DZ will be formed on the boundary shown in F1 of drawing 4 (A). And zener voltage VZ is N+ high impurity concentration (F2 reference.) in this boundary. Concentration of the arsenic As which forms the N+ field 12, and P+ high impurity concentration in this boundary (F3 reference.) It is decided by the concentration of the boron BF 2 which forms the P+ field 16.

[0037] The relation of the P+ high impurity concentration and zener voltage in the case where N+ high impurity concentration is fixed to drawing 5 2.0x1020cm-3 is shown. In order to set zener voltage VZ to 9V as shown in drawing 5 for example, it turns out that what is necessary is just to make P+ high impurity concentration about [3.0x1017cm -] into three. Similarly, in order to set zener voltage VZ to 7V and 5V, it turns out respectively that what is necessary is just to make P+ high impurity concentration into 6.0x1017cm-3 and about [1.0x1018cm -] 3. That is, as P+ high impurity concentration is enlarged, zener voltage VZ becomes smaller.

[0038] Thus, by controlling P+ high impurity concentration, it can adjust now to the value of a request of zener voltage VZ simply.

[0039] 4. gate length — in the example of a background of drawing 1 (A) and (B), gate length L must be

made longer than the base width of face BW as mentioned above. For this reason, gate length L is not made to the lower limit on a design rule. Therefore, in order to heighten the current serviceability of an output transistor, gate width W must be enlarged, and as shown in drawing 6 (A) for this reason, the layout area of an output transistor becomes very large.

[0040] On the other hand, constraint called L>BW can be lost with this operation gestalt. For this reason, gate length L can be made into the lower limit on a design rule. therefore, as shown in drawing 6 (B), the layout area of an output transistor can be markedly boiled compared with drawing 6 (A), and can be made small. Consequently, miniaturization of a semiconductor device and low cost-ization can be attained. since many pads (an output pad, an I/O pad, input pad, etc.) are especially prepared dramatically in a semiconductor device in recent years, if-izing of the layout area of the protection network of a pad can be carried out [small-scale], a chip area is boiled markedly and it comes to be able to make it small

[0041] Moreover, with this operation gestalt, the electrostatic discharge is prevented by discharging a current to a bipolar transistor BP. With the semiconductor device of the type which does not prepare such BP on the other hand, the electrostatic discharge is prevented by discharging a current to the parasitism bipolar transistor BPP at the time of impression of a high-tension pulse. And when the component dimension was not made detailed so much, even if the high current flowed to BPP, the electrostatic discharge of the output transistor was not carried out, but when detailed-ization of a component dimension progressed and gate dielectric film became thin, the situation where the electrostatic discharge of the output transistor is carried out by this high current came to arise. And even if a high current flows to BPP in this way, in order not to carry out the electrostatic discharge of the output transistor, gate length L of an output transistor had to be lengthened.

[0042] And gate length L had to be too lengthened from constraint of L>BW also in the example of a background of drawing 1 (A) and (B) which discharges a current as well as this operation gestalt through BP instead of BPP.

[0043] On the other hand, with this operation gestalt, a current can discharge through BP instead of BPP, and constraint of L>BW can also be lost. For this reason, gate length L could be shortened and it has succeeded in reducing the layout area of an output buffer epoch-makingly.

[0044] 5. It becomes possible to make into the lower limit on a design rule the sizes D1 of the drain contact 40 formed in the drain field 12 as shown in drawing 7 according to [again] this operation gestalt, such as contact size, the distance D2 of the side 41 of the drain contact 40, and the side 44 by the side of the gate electrode 6 of the drain field 12, or the distance D3 grade of the side 42 of the drain contact 40, and the side 46 (it intersects perpendicularly the side 44) of the drain field 12. According to this operation gestalt, it becomes possible similarly to make into the lower limit on a design rule the size D4 of the source contact 50 formed in the source field 10, the distance D5 of the side 51 of the source contact 50, and the side 54 by the side of the gate electrode 6 of the source field 10, or distance D6 of the side 52 of the source contact 50, and the side 56 (it intersects perpendicularly the side 54) of the source field 10. Thereby, the layout area of an output transistor can be further miniaturized now.

[0045] When a high current flows to the parasitism bipolar transistor BPP by high-tension pulse impression, in order to raise ESD susceptibility, it is necessary to enlarge sizes D1 and D4 of the drain contact 40 which is the path for which a current flows, or the source contact 50. Moreover, it is necessary to lengthen distance D2 and D5 and to increase parasitism resistance of the path for which a current flows. Furthermore, it is necessary to lengthen distance D3 and D6 so that an electrostatic discharge may not arise in the parts of the side 46 or the side 56.

[0046] On the other hand, according to this operation gestalt, a current discharges through a bipolar transistor BP instead of the parasitism bipolar transistor BPP at the time of the high-tension pulse impression by ESD. Therefore, even if it shortens D1-D6, for example, makes it the lower limit on a design rule, high ESD susceptibility can be secured. that is, the layout area of an output transistor is boiled markedly and it comes to be able to carry out [****]-izing of it, securing high ESD susceptibility

[0047] 6. Various things can be considered as a gestalt of junction of the gestalt zener diode of junction of zener diode. For example, in drawing 8 (A), the junction J1 of a direction almost parallel to the front face of a semiconductor device among junction of zener diode DZ is narrow. For example, J1 is narrower than the junction J2 of the direction which intersects a front face. With such a junction gestalt, the area of the whole junction with which J1 and J2 were doubled becomes small. For this reason, the leakage current (leakage current which flows from the N+ field 12 to the P well 1 through the P+ field 16) generated in junction can be made small. However, the passage area of the current at the time of high-tension pulse impression may become narrow, and ESD susceptibility may become low. Moreover, the variation width of face of the zener voltage resulting from fluctuation of a manufacture process etc. may become large.

[0048] On the other hand, in drawing 8 (B), the junction J1 of a direction almost parallel to the front face of a semiconductor device among junction of zener diode DZ is large. For example, J1 is larger than the junction J2 of the direction which intersects a front face. With such a junction gestalt, the area of the whole junction with which J1 and J2 were doubled becomes large. For this reason, the leakage current generated in junction will become large. However, the passage area of the current at the time of high-tension pulse impression becomes large, and it becomes possible to raise ESD susceptibility. Moreover, it also becomes possible to reduce the variation in the zener voltage resulting from fluctuation of a manufacture process etc.

[0049] Therefore, in giving priority to control of leakage current, the junction gestalt of drawing 8 (A) becomes advantageous, and in giving priority to improvement in ESD susceptibility, or variation reduction of zener voltage, the junction gestalt of drawing 8 (B) becomes advantageous.

[0050] In addition, the magnitude of junction J1 is controllable by the magnitude of the overlap field IV with the impurity placing field IP for forming the impurity placing field IN and the P+ field 16 for forming the N+ field 12. For example, if the overlap field IV is narrowed as shown in drawing 8 (A), junction J1 will become narrow and J1 will become narrower than junction J2. Thereby, leakage current can be reduced now. On the other hand, if the overlap field IV is made large as shown in drawing 8 (B), junction J1 will become large and J1 will become larger than junction J2. Thereby, while raising ESD susceptibility, the variation in zener voltage can be reduced.

[0051] 7. Explain briefly the manufacture approach, next the manufacture approach of this operation gestalt.

[0052] (1) Manufacture approach 1 drawing 9 (A) The process sectional view of the manufacture approach 1 is shown in - (F).

[0053] The channel stopper layer 62 for the component demarcation membrane (field oxide) 60 and parasitic transistor formation prevention is formed first (drawing 9 (A)). The channel stopper layer 62 is formed by ion implantations, such as boron.

[0054] Next, the gate oxide 64 of desired thickness is formed by thermal oxidation (drawing 9 (B)). And the polish recon film is formed with a CVD method etc., patterning of the polish recon film is carried out according to a photograph process after the ion implantation for threshold adjustment, and the gate electrode 6 is formed (drawing 9 (C)).

[0055] Next, for example, the ion implantation of Lynn which is an N type impurity is carried out by acceleration energy 40KeV and dose 3.0x1013cm-2, and the low concentration impurity ranges 66, 67, and 68 for LDD structure (offset field) are formed (drawing 9 (D)).

[0056] Next, the sidewall 70 for LDD structure is formed. And for example, the ion implantation of the boron which is a P type impurity is carried out by acceleration energy 40KeV and dose 1.2x1013-5.0x1013cm-2, and the P+ field 16 is formed (drawing 9 (E)). In this case, in setting zener voltage as 9V, it makes a dose about [1.2x1013cm -] into two, in setting it as 7V, it carries out to about [3.0x1013cm -] two, and in setting it as 5V, it carries out to about [5.0x1013cm -] two. Moreover, the placing field IP of boron is set up, for example with a given photo mask.

[0057] Next, for example, the ion implantation of the arsenic which is an N type impurity is carried out

by acceleration energy 50KeV and dose 4.0x1015cm−2, and the N+ fields 10, 12, and 14 are formed (drawing 9 (F)). In this case, the placing field IN of an arsenic is set up, for example with a given photo mask.

[0058] In addition, with the formation process of the low concentration impurity range (offset field) of the P type in the LDD structure of a P type transistor, the P+ field 16 can be formed and a process can also be shortened. In this case, it is necessary on the process conditions at the time of forming the low concentration impurity range of P type (dose etc.) to be able to obtain desired zener voltage. Moreover, in this case, before forming the N+ field 12, the P+ field 16 will be formed.

[0059] However, when not forming the P+ field 16 with the formation process of the low concentration impurity range of P type, you may make it form the P+ field 16 after formation of the N+ field 12.

[0060] Furthermore, if desired zener voltage can be obtained, it is also possible to form the P+ field 16 with the formation process of the source field of a P type transistor or a drain field, and to shorten a process.

[0061] By the manufacture approach 1 explained above, as shown in drawing 9 (F), the impurity placing field IN for forming the N+ field 12 and the overlap field IV with the impurity placing field IP for forming the P+ field 16 are narrow. For example, in consideration of the error of mask alignment, it is about 1−2− micrometer overlap. Therefore, although some ESD susceptibility becomes low as drawing 8 (A) already explained, a semiconductor device with little leakage current at the time of normal operation can be offered.

[0062] (2) Manufacture approach 2 drawing 10 (A) The process sectional view of the manufacture approach 2 is shown in − (F).

[0063] In drawing 10 (E), a large point has the difference with the above−mentioned manufacture approach 1 in the placing field IP of the boron which is a P type impurity. Since it is almost the same as that of the manufacture approach 1 about others, detailed explanation is omitted.

[0064] According to the manufacture approach 2, as shown in drawing 10 (F), the impurity placing field IN for forming the N+ field 12 and the overlap field IV with the impurity placing field IP for forming the P+ field 16 become large. Therefore, as drawing 8 (B) already explained, some leakage current at the time of normal operation increases, but while being able to raise ESD susceptibility, the variation in zener voltage can be reduced. (3) Manufacture approach 3 drawing 11 (A) The process sectional view of the manufacture approach 3 is shown in − (F).

[0065] In drawing 11 (E), the point which is driving in the boron which is a P type impurity with the high energy of 100 − 200KeV extent has the difference with the above−mentioned manufacture approach 1. Since it is almost the same as that of the manufacture approach 1 about others, detailed explanation is omitted.

[0066] Since the boron which is a P type impurity is driven in with high energy according to the manufacture approach 3, as shown in drawing 11 (F), it becomes possible to form the P+ field 16 in the field estranged from the front face of a semiconductor device. Thereby, it can prevent now that the P+ field 16 is exposed on the surface of a semiconductor device.

[0067] In addition, this invention is not limited to the above−mentioned operation gestalt, and deformation implementation various by within the limits of the summary of this invention is possible for it.

[0068] For example, this invention is applicable to the protection transistor of the input transistor which can apply not only to an output transistor but to various transistors, for example, is connected to a pad etc.

[0069] Moreover, what [not only] was explained with this operation gestalt but various deformation implementation is possible also for the physical relationship of the 2nd impurity range and the 4th impurity range.

[0070] Moreover, the process conditions at the time of forming an impurity range are not limited to what was explained with this operation gestalt, either.

[0071] Moreover, what [not only] was explained with this operation gestalt but various deformation implementation is possible also for the layout and device structure of a semiconductor device.
[0072] Moreover, although the setting-out technique of zener voltage also has especially the desirable thing explained with this operation gestalt, it is not limited to this.
[0073]

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] Drawing 1 (A) is the top view of a background technique, and drawing 1 (B) is a sectional view in A1-A2 line of drawing 1 (A).
[Drawing 2] Drawing 2 (A) is the top view of this operation gestalt, and drawing 2 (B) is a sectional view in the B1-B-2 line of drawing 2 (A).
[Drawing 3] It is drawing for explaining setting out of zener voltage VZ.
[Drawing 4] Drawing 4 (A) and (B) are drawings for explaining concentration distribution of an impurity.
[Drawing 5] It is drawing showing the relation between P+ high impurity concentration and zener voltage.
[Drawing 6] Drawing 6 (A) and (B) are drawings for explaining the technique of making gate length L the lower limit on a design rule.
[Drawing 7] It is drawing for explaining the technique of making contact size etc. the lower limit on a design rule.
[Drawing 8] Drawing 8 (A) and (B) are drawings showing the various gestalten of junction of zener diode.
[Drawing 9] Drawing 9 (A) - (F) is drawing showing the process sectional view of the manufacture approach 1.
[Drawing 10] Drawing 10 (A) - (F) is drawing showing the process sectional view of the manufacture approach 2.
[Drawing 11] Drawing 11 (A) - (F) is drawing showing the process sectional view of the manufacture approach 3.
[Description of Notations]
1 P Well
2 Output Transistor
4 Bipolar Transistor
6 Gate Electrode
10 N+ Field (1st Impurity Range)
12 N+ Field (2nd Impurity Range)
14 N+ Field (3rd Impurity Range)
16 P+ Field (4th Impurity Range)
20, 22, 24, 26 Wiring layer
28 P+ Field

30 Pad
32 High-Tension Pulse
40 Drain Contact
41, 42, 44, 46 Side
50 Source Contact
51, 52, 54, 56 Side
60 Component Demarcation Membrane
62 Channel Stopper Layer
66, 67, 68 Low concentration impurity range
70 Sidewall
201 P Well
202 Output Transistor
204 Bipolar Transistor
206 Gate Electrode
210 N+ Field
212 N+ Field
214 N+ Field
220, 222, 224, 226 Wiring layer
228 P+ Field
230 Pad
232 High-Tension Pulse
DZ Zener diode
DA Parasitism diode
BP Bipolar transistor
BPP Parasitism bipolar transistor

[Translation done.]